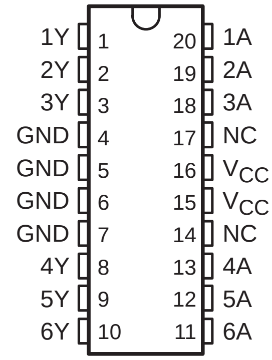
- **Replaces 74AC11203**
- **Low-Skew Propagation Delay Specifications for Clock Driver Applications**
- **Operates at 3.3-V V_{CC}**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Pin Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-µm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Packaged in Plastic Small-Outline Package**

DW PACKAGE
(TOP VIEW)



NC – No internal connection

description

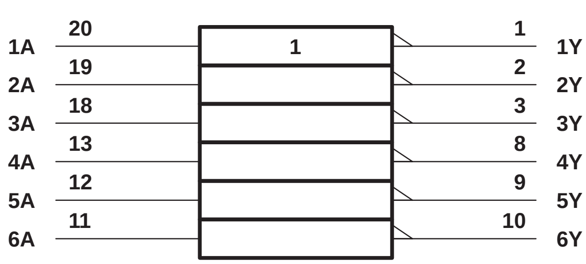
The CDC203 contains six independent inverters. The device performs the Boolean function $Y = \overline{A}$. It is designed specifically for applications requiring low skew between switching outputs.

The CDC203 is characterized for operation from 25°C to 70°C.

FUNCTION TABLE

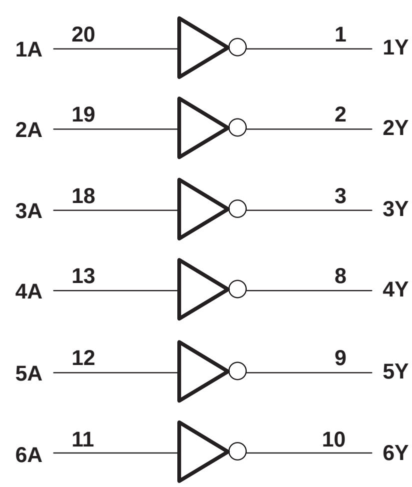
INPUT A	OUTPUT Y
H	L
L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . ±150 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2) . . . . 1.6 W
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 3.6 V	2.5			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 3.6 V			1.1	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			–12	mA
		V_{CC} = 3.6 V			–12	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 3.6 V			12	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
f_{clock}	Input clock frequency				40	MHz
T_A	Operating free-air temperature		25		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

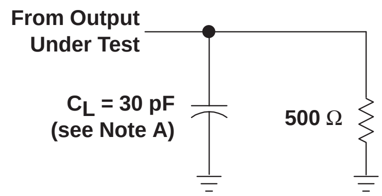
PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C MIN	T_A = 25°C TYP	T_A = 25°C MAX	MIN	MAX	UNIT
V_{OH}	I_{OH} = – 50 µA	3 V	2.9			2.9		V
		3.6 V	3.5			3.5		
	I_{OH} = – 12 mA	3 V	2.58			2.48		
		3.6 V	3.18			3.08		
V_{OL}	I_{OL} = 50 µA	3 V			0.1		0.1	V
		3.6 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
		3.6 V			0.36		0.44	
I_I	$V_I = V_{CC}$ or GND	3.6 V			±0.1		±1	µA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			4		40	µA
C_i	$V_I = V_{CC}$ or GND	3.3 V		4				pF

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (see Note 3 and Figures 1 and 2)

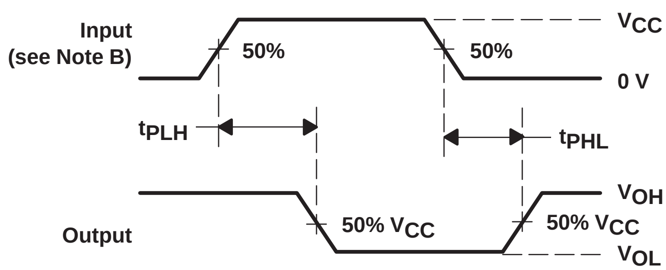
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{PLH}	A	Y	3.5	6.1	ns
t_{PHL}			3.5	6.1	
$t_{sk(o)}$	A	Y		0.7	ns

NOTE 3: All specifications are valid only for all outputs switching in phase simultaneously.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

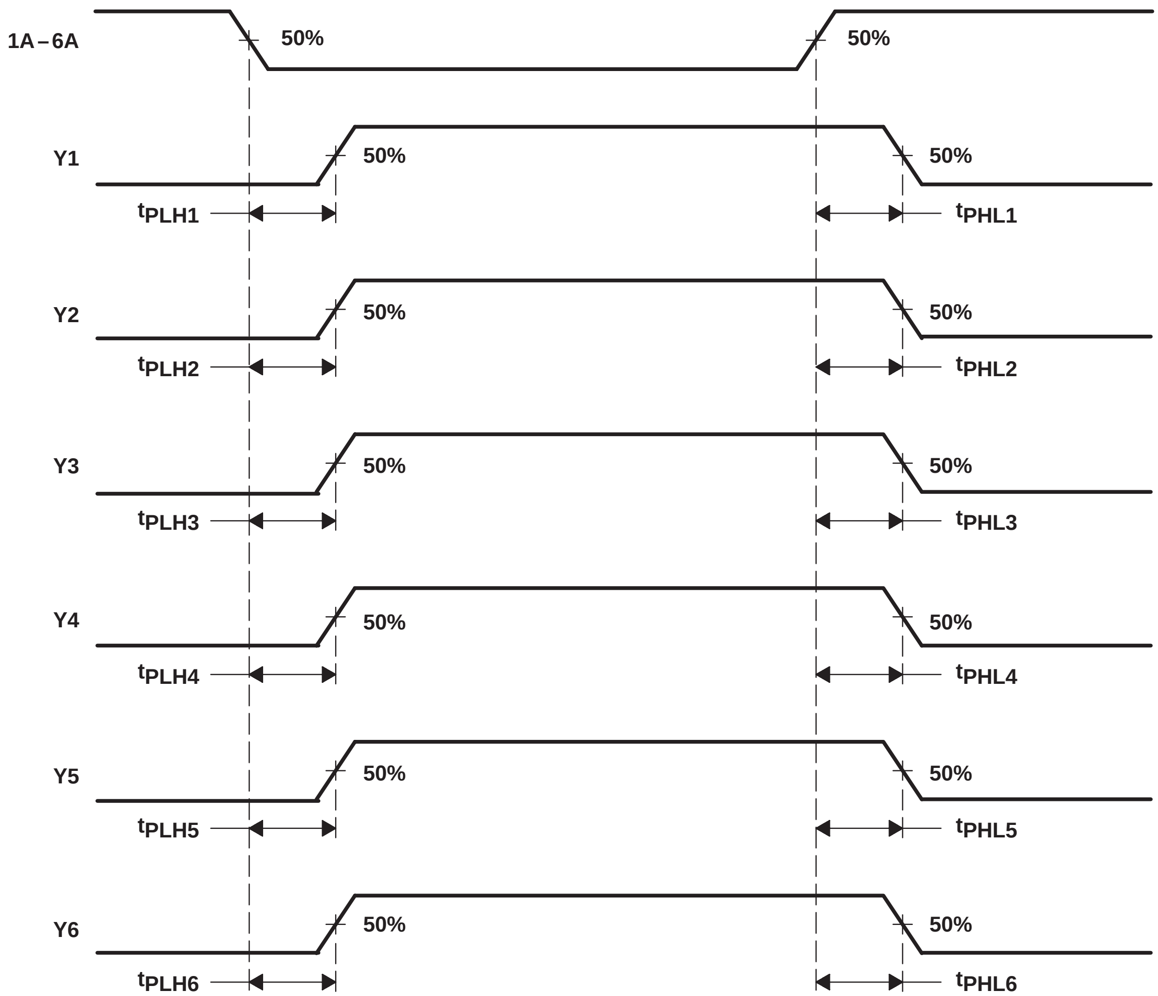


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2, . . . , 6)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2, . . . , 6)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

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